XA-9472
PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Yasuhisa SHIMAZAKI et al.

Appln. No.:

Filed: Herewith

For: SEMICONDUCTOR INTEGRATED CIRCUIT

* * *

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination, please amend the above-identified application as indicated below.

IN THE CLAIMS:

8. (Amended) A semiconductor integrated circuit according to claim 6, wherein said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by a potential in said well region, and said second logic gate includes an MIS transistor to which a substrate bias is applied in a forward direction by a potential in said well region.

9. (Amended) A semiconductor integrated circuit according to claim 6, wherein said first logic gate includes a

p-channel type MIS transistor and an n-channel type MIS transistor to which a substrate bias is applied in a reverse direction by the potential of said well region, and said second logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which a substrate bias is applied in a forward direction by a potential of said well region.

10. (Amended) A semiconductor integrated circuit according to claim 6, wherein said first logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a reverse direction by a potential of said well region, and said second logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a forward direction by a potential in said well region.

11. (Amended) A semiconductor integrated circuit according to claim 6, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which a substrate bias is applied in a reverse direction by a potential in said well region.

Please add the following new claims:

39. (New) A semiconductor integrated circuit according to claim 7, wherein said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse

direction by a potential in said well region, and said second logic gate includes an MIS transistor to which a substrate bias is applied in a forward direction by a potential in said well region.

40. (New) A semiconductor integrated circuit according to claim 7, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which a substrate bias is applied in a reverse direction by the potential of said well region, and said second logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which a substrate bias is applied in a forward direction by a potential of said well region.

41. (New) A semiconductor integrated circuit according to claim 7, wherein said first logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a reverse direction by a potential of said well region, and said second logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a forward direction by a potential in said well region.

42. (New) A semiconductor integrated circuit according to claim 7, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to

which a substrate bias is applied in a reverse direction by a potential in said well region.

REMARKS

The multiple dependencies have been eliminated from Claims 8-11 to avoid the surcharge for multiple dependent claims, see the accompanying hand-marked version. Claims 39-42 correspond to the dependencies eliminated from Claims 8-11.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

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said first logic is formed and a well region of the MIS transistor in which said second logic gate is formed are made common every conduction type.

7. A semiconductor integrated circuit comprising:

a first logic gate using, as an operation power source, a first pair of potentials having a relatively small potential difference; and

a second logic gate using, as an operation power source, a second pair of potentials having a relatively large potential difference,

wherein each of said first and second logic gates has an MIS transistor, and a well region of the MIS transistor in which said first logic gate is formed and a well region of the MIS transistor in which said second logic gate is formed are electrically made conductive every conduction type.

8. (Amended) A semiconductor integrated circuit according to claim 6 [or 7], wherein said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by a potential in said well region, and said second logic gate includes an MIS transistor to which a substrate bias is applied in a forward direction by a potential in said well region.

9. (Amended) A semiconductor integrated circuit according to claim 6

[or 7], wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which a substrate bias is applied in a reverse direction by the potential of said well region, and said second logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which a substrate bias is applied in a forward direction by a potential of said well region.

(Amended)
10. A semiconductor integrated circuit according to claim 6 [or 7], wherein said first logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a reverse direction by a potential of said well region, and said second logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a forward direction by a potential in said well region.

(Amended)
11. A semiconductor integrated circuit according to claim 6 [or 7], wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which a substrate bias is applied in a reverse direction by a potential in said well region.

12. A semiconductor integrated circuit comprising:

a first logic gate using, as an operation power source, a first pair of a high potential and a low potential; and